



H-1018-03

Prior Application: N. TAKAHASHI et al  
Serial No. 10/453,606  
Filed: June 4, 2003

Group Art Unit: 2813  
Examiner: C. Chaudhari  
For: A METHOD OF MANUFACTURING A  
SEMICONDUCTOR DEVICE AND A  
SEMICONDUCTOR DEVICE

17548 U.S. PTO  
10/784276

February 24, 2004

Basic Fee						\$ 770.00
Total Claims	15 -	20 =	0 x	18 =		\$ 0.00
Independent Claims	2 -	3 =	0 x	86 =		\$ 0.00
Total Filing Fee						<u>\$ 770.00</u>

## CONTINUATION APPLICATION

H-1018-03

3. A credit card payment form including the amount of \$770.00 is enclosed to cover the Filing Fee.

4. The Commissioner is hereby authorized to charge any additional fees which may be required, or to credit any overpayment, to Deposit Account No. 50-1417.

5. New drawings are enclosed, forty-one (41) sheets, Figs. 1-47(b).

6. The power of attorney is set forth in the Declaration in the prior application or an associate power of attorney is hereby granted to:

Jeffrey M. Ketchum, Registration No. 31,174  
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There is no change in the correspondence address.

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**Please associate this application with Customer No. 24956.**


7. The prior application is assigned to Renesas Technology Corp., Hitachi ULSI Systems Co., Ltd., and Hitachi Yonezawa Electronics Co., Ltd.

8. Priority of the following Japanese patent application is claimed under 35 U.S.C. § 119:

No. 2000-387825, filed December 20, 2000.

The certified priority document has been filed in the parent application Serial No. 09/987,532.

The undersigned hereby declares that no matter contained in the specification, including the claims, and drawings filed in the present continuation application would have been new matter in the prior application Serial No. 10/453,606, as originally filed on June 4, 2003.

  
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